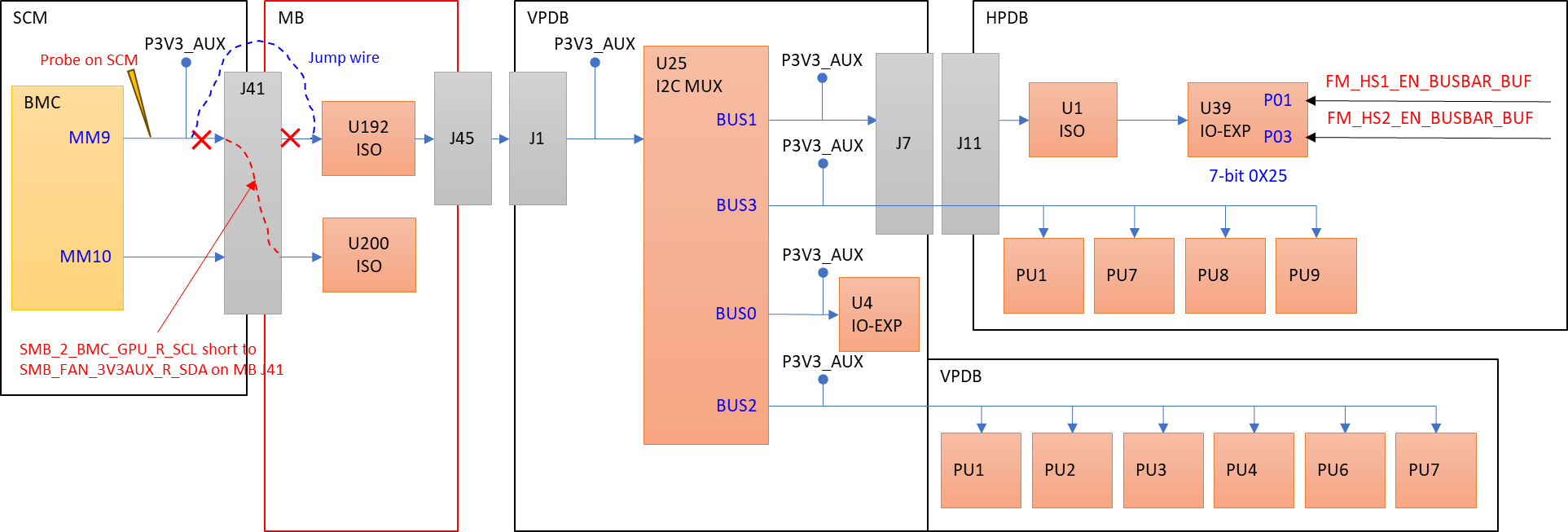
1. Type C connector對地短路事件

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| Case 1 | |
|  | Artemis Jira-538 |
| Situation | UART Bridges missed in BmcUSBCountCheck of FFT during PVT build.  FR is 0.46% in MP stage |
| Task | Solving UART bridge missing Issue since PVT stage |
| Action | 1. Check “select pin”, found that it was short to GND without USB plug in. 2. Cut connection to find the shorting point. 3. Seem’s the “short” is on the Type C connector. 4. Sink current into this pin can fix the short. 5. Re-mount also can fix it. -> looked like mounting issue. 6. Do X-ray and board slice to check, but can’t find the shorting path. 7. Analyze manufacture build info, the issue only occurred on “Lotus”. 8. Conduct a full inspection of the "Lotus" connector before the PCBA build. The defects were found in the material before the SMT process. 9. RMA the defected connector. And ask for improvement  plan. |
| Result | The issue was caused by a defective connector. The vendor helped fix it and then allowed it to be returned for production. |

1. PDB Log 誤報事件

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| Case 2 | |
|  | Artemis Jira-183 |
| Situation | After sled cycle, that have chance will record "Record time delay 300ms, FRU: 1 , enable HPDB\_HS1\_BUSBAR\_EN" in bmc sel |
| Task | Investigate the root cause of issue log |
| Action | 1. Replicate the issue overnight, can be reproduce easily. 2. Measure on the issue net, but scope can’t capture it when issue occurred. 3. The issue FR is positive relation to the BMC pulling frequency. ->Should be related to I2C bus. 4. Check I2C signal, found that when issue occurred, the “SDA” seems to be “Change to CLOCK”. 5. Check i2c path, found that the “SDA” net short to “SCL” of others I2C BUS. |
| Result | The issue cause by the defected 4C+ connector. And it’s single case. |

“附圖展示當初找到short的位置”



1. BUSBAR事件

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| Case 3 | |
|  | Artemis Jira-640 |
| Situation | [MP] System intermittently encountered unexpected reboot or HPDB power fault during L10 testing |
| Task | Find the root cause of the unexpected reboot |
| Action | 1. The issue seemed random in the early stages and did not follow a specific PCBA, L10, or rack. 2. No conclusion was reached after extensive swap testing. 3. The factory site reviewed security camera footage and found that the issue always occurred when an operator inserted or removed another L10 in the same rack. 4. Suspected a power pin mating issue between the L10 and the rack BUSBAR. 5. On-site signal measurements revealed voltage jitter on the "sense pin" when inserting the bottom L10 while measuring on the top L10. |
| Result | Since the Artemis L10 is heavier than other projects, and there were only three L10 units in one rack, the vibration during insertion or removal of the L10 has a greater impact than in other projects. Therefore, it is necessary to lower the sensitivity of the BUSBAR monitor sense pin. (Increase the filter capacitance) |

“推最底層L10進入時，上層L10抓到的signal drop”

